What is Claimed is:

1. A method for forming a floating gate for a flash memory device in a semiconductor assembly, comprising the steps of:

forming a tunnel oxide with openings therein to expose underlying silicon;

forming an epitaxial silicon layer over said tunnel oxide by using said exposed underlying silicon as a silicon seeding source; and

patterning said epitaxial silicon layer into said floating gate.

2. The method of claim 1, wherein said step of forming an epitaxial silicon layer further comprises depositing epitaxial silicon.

3. The method of claim 1, wherein said step of forming an epitaxial silicon layer further comprises using solid phase epitaxy of a deposited amorphous silicon layer.

4. The method of claim 1, wherein said step of forming an epitaxial silicon layer further comprises conductively doping said epitaxial silicon layer.

5. The method of claim 4, wherein said step of conductively doping said epitaxial silicon layer comprises insitu doping.

6. The method of claim 4, wherein said step of conductively doping said epitaxial silicon layer comprises ion implant doping.

7. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a tunnel oxide with openings therein to expose underlying silicon;

forming an epitaxial silicon layer over said tunnel oxide by using said exposed underlying silicon as a silicon seeding source;

forming an inner-dielectric layer over said epitaxial silicon layer;

forming a polycide layer over said inner-dielectric layer;

forming transistor gates from said polycide layer, said inner-dielectric layer, said epitaxial silicon layer and said tunnel oxide; and

forming source and drain electrodes on opposing sides of said transistor gates.

8. The method of claim 7, wherein said step of forming an epitaxial silicon layer further comprises depositing epitaxial silicon.

9. The method of claim 7, wherein said step of forming an epitaxial silicon layer further comprises using solid phase epitaxy of a deposited amorphous silicon layer.

10. The method of claim 7, wherein said step of forming an epitaxial silicon layer further comprises conductively doping said epitaxial silicon layer.

11. The method of claim 10, wherein said step of conductively doping said epitaxial silicon layer comprises insitu doping.

12 The method of claim 10, wherein said step of conductively doping said epitaxial silicon layer comprises ion implant doping.

13. A floating gate for a flash memory device in a semiconductor assembly, comprising:

an epitaxial silicon floating gate overlying a tunnel oxide by using said exposed underlying silicon as a silicon seeding source.

14. The floating gate of claim 13, wherein said epitaxial silicon floating gate comprises conductive ions.

15. A flash memory device in a semiconductor assembly, comprising:

an epitaxial silicon floating gate containing conductive ions and overlying a tunnel oxide material;

an inner-dielectric material overlying said epitaxial silicon floating gate

a polycide material over said inner-dielectric material, said tunnel oxide material, said epitaxial silicon floating gate, said inner-dielectric material and said polycide material forming a transistor gate; and

source and drain electrodes on opposing sides of said transistor gate.